DOCKET NO.: MSFT-1794 / 303770.1 **PATENT**

Application No.: 10/622,597 Office Action Dated: 02/07/2005

REMARKS

Status of the Claims

- Claims 1-29 are pending in the Application.
- Claims 1-28 are rejected by Examiner.
- Claims 1, 13, 22 and 28 are amended by Applicant.
- Claim 8 is cancelled without prejudice or disclaimer.
- Claim 29 is added by Applicant.

Claim Rejections Pursuant to 35 U.S.C. §112 First Paragraph

Claim 8 stands rejected pursuant to 35 U.S.C. §112 first paragraph as failing to particularly point out and distinctly claim the subject matter which application regards as his invention. Applicants have cancelled Claim 8 without prejudice or disclaimer.

Claim Rejections Pursuant to 35 U.S.C. §102

Examiner has rejected Claims 1-28 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 2002/0196256 to Hoppe et al. Applicants respectfully traverse the §102(e) rejection.

Hoppe et al. teaches a system and method to effect the reduction of aliasing artifacts along discontinuity edges of a rendered polygon mesh by overdrawing the edges as antialiased lines. The processes of Hoppe et al. are targeted to be effective at reducing the temporal artifact known as "crawling jaggies". (Abstract)

Claim 1 recites a method for rendering graphics on a display device for a computer system. The method includes rendering a graphic in the system random access memory with the central processing unit and copying said graphic from the system random access memory directly into the frame buffer.

Hoppe et al. teaches that a rendering module 240, within the graphics processing unit 206 of Figure 2, renders partial images into the frame buffer 208. Specifically, Hoppe et al. teaches at paragraph 0040 and paragraph 0053:

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[0040] The GPU 206 includes a rendering module 240 and an overdrawing module 242, which can be implemented in hardware or a combination of hardware and software. The rendering module 240 renders the triangles from the mesh 232 and places the rendered images in the frame buffer 208.

[0053] At block 406, the rendering module 240 of the graphics processing unit 206 renders an image as a triangle mesh (or other polygon mesh). For efficiency, it is specified as a display list of triangle strips. The z-buffer is used to resolve occlusion, and is saved for use during edge overdraw. The image is placed in the frame buffer 208.

Hoppe et al. fails to teach rendering a graphic in the system random access memory with the central processing unit and copying said graphic from the system random access memory *directly into the frame buffer*.

Since Hoppe et al. fails to teach or suggest rendering a graphic in the system random access memory with the central processing unit and copying said graphic from the system random access memory directly into the frame buffer, it cannot anticipate amended independent Claim 1.

Accordingly, Applicant respectfully requests withdrawal of the §102(e) rejection and submits that amended independent Claim 1 patentably defines over the cited art. Similarly, independent Claims 13, 22 and 28 are amended to also recite rendering a graphic in the system random access memory with the central processing unit and copying a graphic from the system random access memory directly into the frame buffer. Applicant respectfully requests withdrawal of the §102(e) rejection of amended independent Claims 1, 13, 22 and 28 because they patentably define over the cited art. Applicant also respectfully requests withdrawal of the §102(e) rejection on the respective dependent claims as they also patentably define over Hoppe et al.

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Conclusion

In view of the above amendments and remarks, Applicant submits that the present application is in a condition for allowance upon entry of the amendments herein.

Applicant respectfully and earnestly solicits a Notice of Allowance for all pending claims.

Respectfully submitted,

PATENT

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